

In the Claims:

Please amend claims 3-5 and 13-15. The claims are as follows:

1. (Original) An electrical structure, comprising:

a dielectric substrate having a metal signal line therein; and

a first metal voltage plane laminated to a first surface of the dielectric substrate, wherein the first metal voltage plane includes an opening, wherein an image of a first portion of the metal signal line projects across the opening in the first metal voltage plane, and wherein a first electrically conductive strip across the opening in the first metal voltage plane includes the image of the first portion.

2. (Original) The electrical structure of claim 1, wherein the first electrically conductive strip is integral with the first metal voltage plane.

3. (Currently amended) ~~The electrical structure of claim 1~~ An electrical structure, comprising:

a dielectric substrate having a metal signal line therein; and

a first metal voltage plane laminated to a first surface of the dielectric substrate, wherein the first metal voltage plane includes an opening, wherein an image of a first portion of the metal signal line projects across the opening in the first metal voltage plane, and wherein a first electrically conductive strip across the opening in the first metal voltage plane includes the image of the first portion, wherein the first electrically conductive strip is not integral with the first

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metal voltage plane.

4. (Currently amended) The electrical structure of claim ~~[[1]]~~ 2, wherein the first electrically conductive strip is ~~linear across the opening in~~ does not extend above or below the first metal voltage plane.

5. (Currently amended) ~~The electrical structure of claim 1~~ An electrical structure, comprising:
a dielectric substrate having a metal signal line therein; and
a first metal voltage plane laminated to a first surface of the dielectric substrate, wherein
the first metal voltage plane includes an opening, wherein an image of a first portion of the metal
signal line projects across the opening in the first metal voltage plane, and wherein a first
electrically conductive strip across the opening in the first metal voltage plane includes the image
of the first portion, wherein the first electrically conductive strip is nonlinear across the opening
in the first metal voltage plane.

6. (Original) The electrical structure of claim 1, wherein the opening in the first metal voltage plane has a vent area of no less than about 0.1 square millimeters.

7. (Original) The electrical structure of claim 1, wherein a signal current is flowing through the metal signal line, wherein a return current is flowing through the first electrically conductive strip, wherein the signal current is an alternating current, and wherein the return current includes a portion of the signal current.

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8. (Original) The electrical structure of claim 1, wherein the electrical structure comprises an electrical apparatus selected from the group consisting of a chip carrier and a printed circuit board, and wherein the electrical apparatus includes the dielectric substrate and the metal voltage plane.

9. (Original) The electrical structure of claim 1, further comprising:

a second metal voltage plane laminated to a second surface of the dielectric substrate, wherein the second metal voltage plane includes an opening, wherein an image of a second portion of the metal signal line projects across the opening in the second metal voltage plane, and wherein a second electrically conductive strip across the opening in the second metal voltage plane includes the image of the second portion.

10. (Original) The electrical structure of claim 9, wherein a signal current is flowing through the metal signal line, wherein a first return current is flowing through the first electrically conductive strip, wherein a second return current is flowing through the second electrically conductive strip, wherein the signal current is an alternating current, wherein the first return current includes a first portion of the signal current, and wherein the second return current includes a second portion of the signal current.

11. (Original) A method for forming an electrical structure, comprising:

providing a dielectric substrate having a metal signal line therein;

laminating a first metal voltage plane to a first surface of the dielectric substrate; and

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forming an opening in the first metal voltage plane such that a first electrically conductive strip across the opening includes an image of a first portion of the metal signal line, wherein the image of the first portion of the metal signal line projects across the opening in the first metal voltage plane.

12. (Original) The method of claim 11, wherein the first electrically conductive strip is integral with the first metallic voltage plane.

13. (Currently amended) ~~The method of claim 11~~ A method for forming an electrical structure, comprising:

providing a dielectric substrate having a metal signal line therein;
laminating a first metal voltage plane to a first surface of the dielectric substrate; and
forming an opening in the first metal voltage plane such that a first electrically conductive strip across the opening includes an image of a first portion of the metal signal line, wherein the image of the first portion of the metal signal line projects across the opening in the first metal voltage plane, wherein the electrically conductive strip is not integral with the first metallic voltage plane.

14. (Currently amended) The method of claim ~~[[11]]~~ 12, wherein the first electrically conductive strip is ~~linear across the opening in~~ does not extend above or below the first metal voltage plane.

15. (Currently amended) ~~The method of claim 11~~ A method for forming an electrical structure,

comprising:

providing a dielectric substrate having a metal signal line therein;
laminating a first metal voltage plane to a first surface of the dielectric substrate; and
forming an opening in the first metal voltage plane such that a first electrically conductive
strip across the opening includes an image of a first portion of the metal signal line, wherein the
image of the first portion of the metal signal line projects across the opening in the first metal
voltage plane, wherein the first electrically conductive strip is nonlinear across the opening in the
first metal voltage plane.

16. (Original) The method of claim 11, wherein the opening in the first metal voltage plane has a vent area of no less than about 0.1 square millimeters.

17. (Original) The method of claim 11, further comprising:

flowing a signal current through the metal signal line, wherein the signal current is an alternating current; and

flowing a return current through the first electrically conductive strip, wherein the return current includes a portion of the signal current.

18. (Original) The method of claim 11, further comprising:

laminating a second metal voltage plane to a second surface of the dielectric substrate;
and

forming an opening in the second metal voltage plane such that a second electrically

conductive strip across the opening includes an image of a second portion of the metal signal line, wherein the image of the second portion of the metal signal line projects across the opening in the second metal voltage plane.

19. (Original) The method of claim 18, further comprising:

flowing a signal current through the metal signal line, wherein the signal current is an alternating current;

flowing a first return current through the first electrically conductive strip, wherein the first return current includes a first portion of the signal current; and

flowing a second return current through the second electrically conductive strip, wherein the second return current includes a second portion of the signal current.

20. (Original) A method for designing an electrical structure that includes a dielectric laminate, said method comprising:

designing the dielectric laminate to include at least one dielectric substrate and at least one metal voltage plane, wherein a first metal voltage plane of the at least one metal voltage plane is laminated to a first dielectric substrate of the at least one dielectric substrate;

determining where in the at least one metal voltage plane to place openings for venting of gases generated during fabrication of the dielectric laminate;

determining at least one problematic opening of the openings, wherein the at least one problematic opening is above or below a corresponding metal signal line within the dielectric laminate such that an image of a portion of the corresponding metal signal line projects across

the at least one problematic opening; and

designing the at least one problematic opening to include an electrically conductive strip across the at least one problematic opening, wherein the electrically conductive strip includes the image.

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